DVCon Panel “SoC Verification Challenges”

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Do New SoC Architectures Demand New Tools and Approaches ?

Panel

- Nirmal Aramugam – QCOM – Mobile SoC Verification Lead
- Sukamar Raghuram – Intel Server Verification Lead
- Pankaj Kakkar – Cadence - Systems and Verification Product Engineering

What Functional Challenges are you facing ?

- QCOM
  - Cloud and Edge driving big data
    - Growing significance of AI engines
    - Workloads very unpredictable – hence need for Traffic Modelling to simulate Video, Audio and more
    - Performance Validation with these synthetic workloads is key
  - Camera demands in Mobile are significant
    - 3 cameras, with image stabilization
    - Augmented reality puts huge demands on data processing
  - Coherency across all these compute engines
    - Big-LITTLE is accepted standard
- Intel
  - System-level distributed compute model is a good one, but demands rigorous verification
  - Bare-bones coherency verification is significant
    - So many engines and interfaces sharing data
  - Performance Validation is a huge challenge
    - Validating architectural performance on RTL models requires complex use-cases
  - Power Management
    - Centralized power controllers, PHYs

What Resource Challenges are you facing ?

- Given the growing complexity are the resources/timescales scaling proportionally ?
  - Human Capital
    - Need to have a bug budget
    - Broader range of tools beyond simulation
  - Machine budget
    - Formal, HW Acceleration
    - Need lowest bring-up cost, and efficient usage across more than just simulation
    - Need partnership between IP and SoC verification teams
    - Need partnership between EDA and SoC developers
  - 3DIC
    - Will drive more resource demands
    - Seeing 2-4X compute resource growth per year (Nirmal)

New Approaches to Address the Challenges ?
PSS

- QCOM very early adopters of Portable Stimulus Standard (PSS)
  - Mostly used for project-to-project reuse of SoC workloads
  - Not currently used for IP to SoC
  - Methodology is still in evolution stage
- Intel
  - SystemVerilog has had a huge impact on IP verification
  - PSS will be similarly impactful
    - especially in constructing scenarios to reuse scenarios from architecture to RTL
  - Broad adoption is the goal, still evolving across projects
- Cadence
  - Bringing in the test intent early as part of the modelling is key
    - Allows definition of SoC coverage to measure progress
    - Works across multiple platforms
  - Portability across UVM to SW-driven testing is a big value

New Approaches to Address the Challenges ?
HW Platforms

- QCOM
  - Security verification is a big challenge and requires HW-SW validation, needs to run on HW
  - Always-on camera, needed for face recognition unlocking.
    - Validating correct function was extremely complex as multiple engines and SW needed, had to be done on HW Acceleration
  - Hybrid (Compute Subsystem in TLM connected to HW) delivers the speed needed for certain use-cases.
- Intel
  - Hybrid models used extensively
    - Efficient both in capacity and performance

New Approaches to Address the Challenges ?
Machine Learning

- QCOM
  - Regression management is a key area where ML can play a role
  - Stimulus management also could be a useful area
  - Failure analysis with ML is useful, in-house tools – looking to EDA to commercialize
  - Expert system for debug
- Intel
  - Verification is “tailor-made” for ML .. lots of in-house ML tools
  - Regression optimization
  - Debug smarter
  - Using past projects to predict regression for next project
    - Regression prediction
    - Bug prediction
    - Coverage prediction
    - Which tests to run on GLS ? Can ML help solve this tough problem ?

New Approaches to Address the Challenges ?
Formal

- Intel
  - Used formal for very specific SoC verification items
    - Bug classification can help reduce the amount of simulation needed
    - Get micro architecture guys bought in to using formal
- QCOM
  - Mostly use SEQ for late ECO checking
  - Low Power connectivity using formal
  - Power Domain validation against hierarchical CPF
- What happened to the dream of automating SoC assembly ?
  - Was a vision about 10 years ago but hasn't been realized
    - This was confirmed, some companies looked into this but the complexities really haven't been solved.

Summary

- SoC Verification Challenges are Significant and growing
  - Coherency challenges are pervasive and complex
  - Performance Verification is increasing important and done at RTL
  - Low Power and Security all add to the challenge
- Resources are always limited and hence smart approaches and tools are essential
  - Verification Management becomes front and central to optimization utilization of resources
    - Cloud and On-Premises mixing
    - Using Machine Learning to harvest data during a project
    - Using Machine Learning to harvest data project to project
  - Creating complex SoC Scenarios with PSS is becoming mainstream
    - Use-case creation is needed for Coherency, Low Power, security and more
  - HW Acceleration is ubiquitous and critically important
    - Innovative use-models like Hybrid are improving ROI
  - Formal can be useful for very specific SoC challenges