
# OpenHW Group

## Proven Processor IP

# CORE-V-VERIF:

## An Industrial-Grade Verification Platform for RISC-V Cores

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OPENHW GROUP™ and CORE-V™

PROVEN PROCESSOR IP


- OpenHW Group is a not-for-profit, global organization driven by its members and individual contributors where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the CORE-V Family of open-source RISC-V cores.

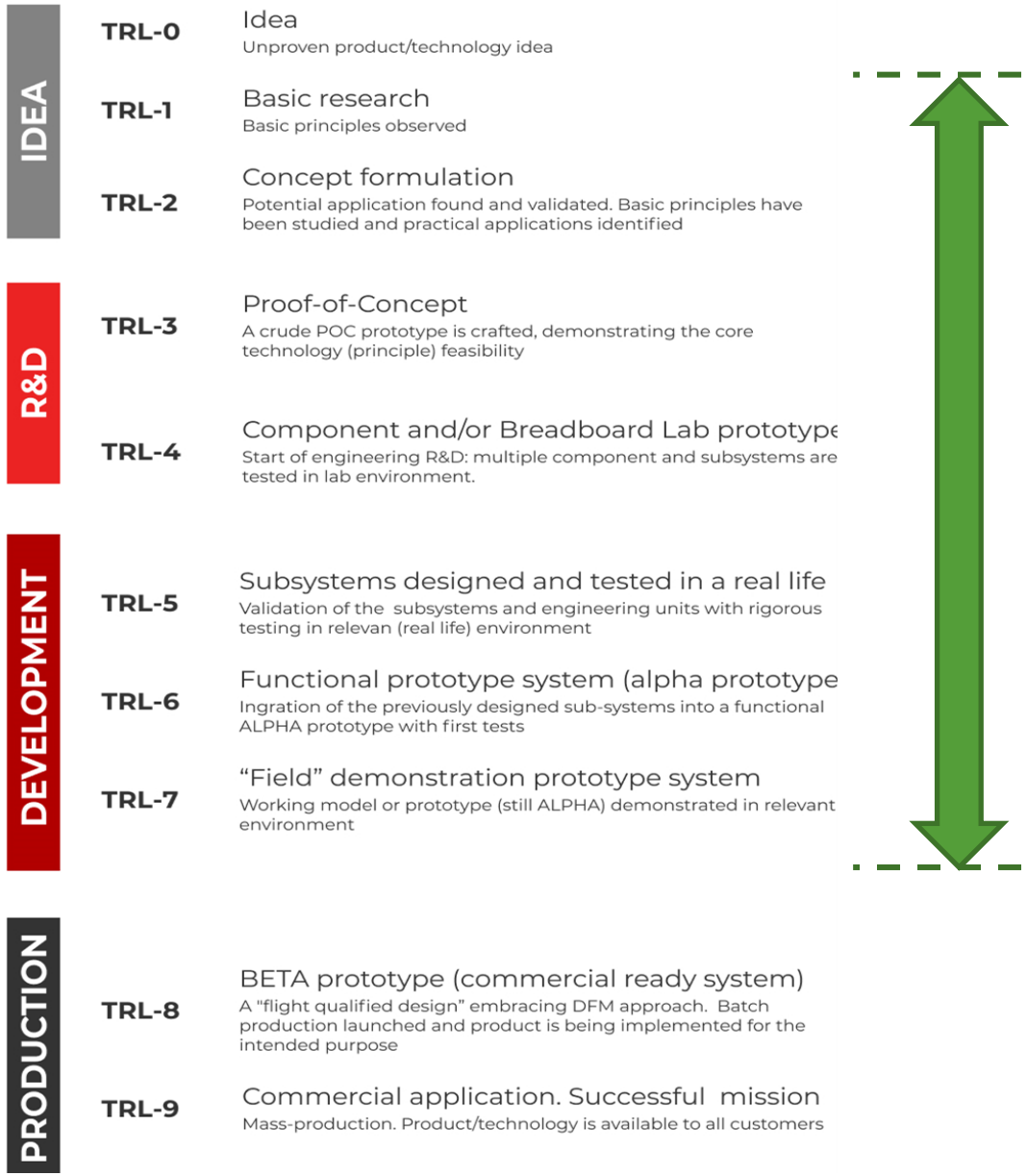
  - International footprint with developers in North America, Europe and Asia.
  - Providing an infrastructure for hosting high quality open-source HW developments in line with industry best practices.
  - Strong support from industry, academia and individual contributors worldwide.

# Industry Ecosystem
# 90+ Members & Partners

Member companies provide human, compute and tool resources.


Open source code base administered on GitHub.

# Technology Readiness Levels




OpenHW Technology Outputs

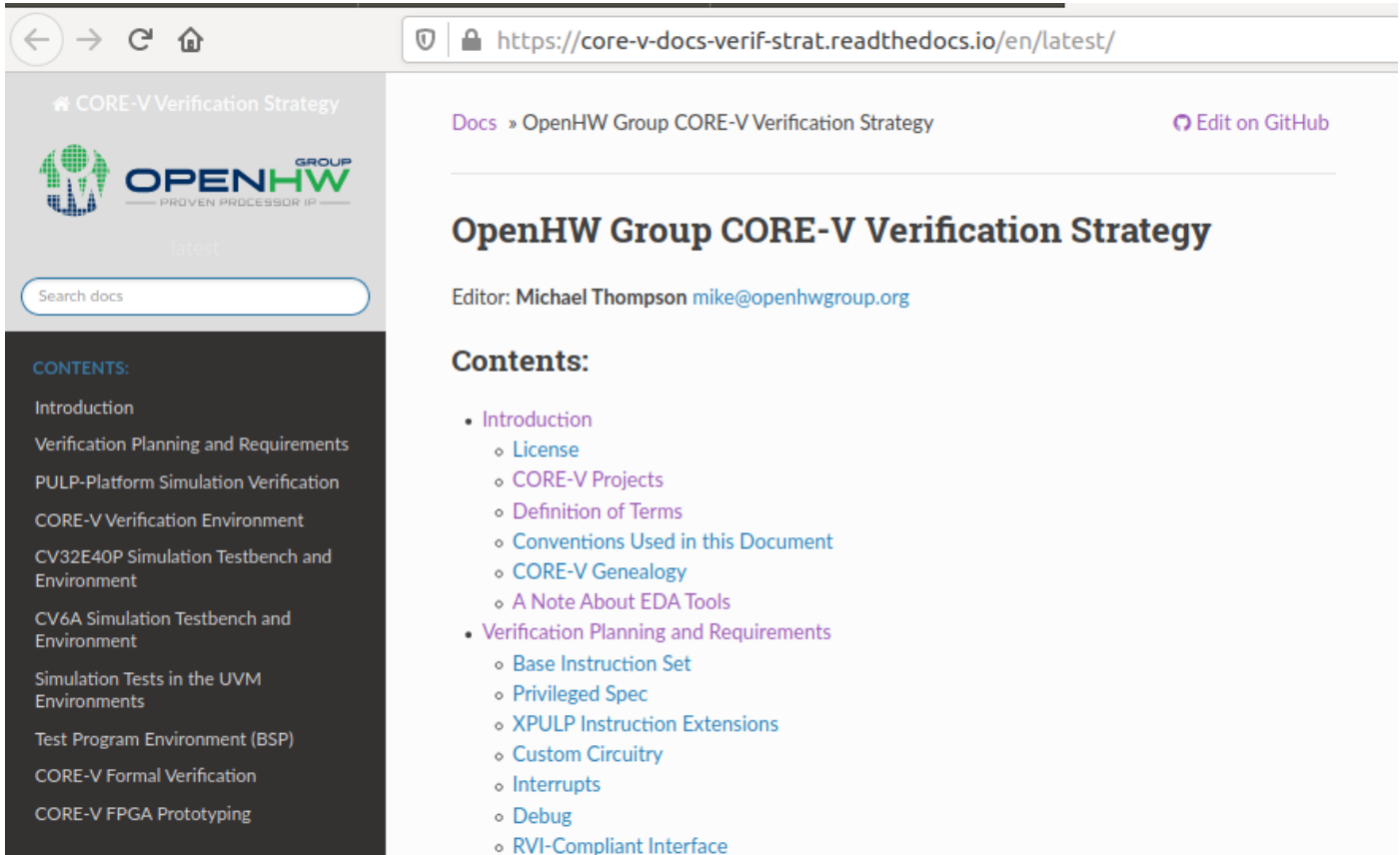
OpenHW IP Adopters

# Verification Task Group Mandate

- From the CORE-V Verification Strategy:
  - *The OpenHW Group will, together with its Member Companies, execute a complete, industrial grade pre-silicon verification of the first generation of CORE-V IP, the CV32E4 and CVA6 cores. Experience has shown that "complete" verification requires the application of both dynamic (simulation, FPGA prototyping, emulation) and static (formal) verification techniques. All of these techniques will be applied to both CV32E4 and CVA6.*

Some big statements made here:

- Complete, industrial grade pre-silicon verification.
- Simulation, Formal and FPGA prototyping.



# Open Source Implementations
## ...but not necessarily open source tools

- In order to achieve “complete, industrial grade verification”, industrial quality tools are used.
- CORE-V-VERIF UVM Verification verification environment runs on all of the major commercial SystemVerilog simulators

ALDEC THE DESIGN VERIFICATION COMPANY

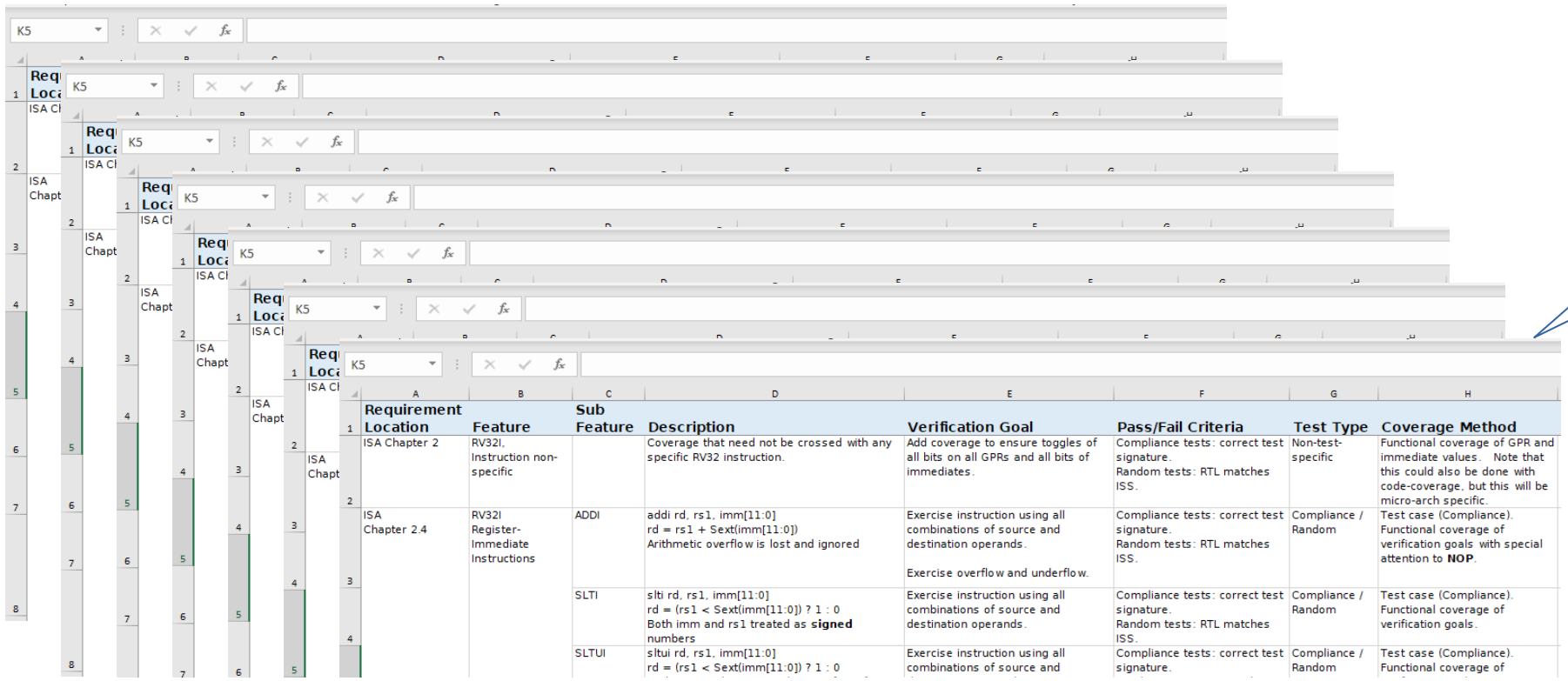
cadence

Mentor A Siemens Business

metrics

SYNOPSYS

# Verification Planning



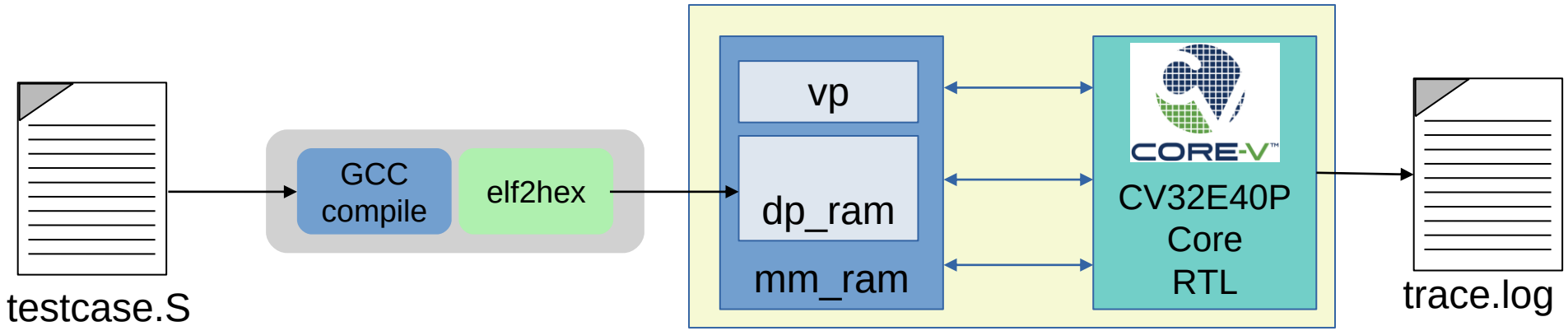
| Requirement Location | Feature | Sub Feature | Description | Verification Goal | Pass/Fail Criteria | Test Type | Coverage Method |
|---|---|---|---|---|---|---|---|
| ISA Chapter 2 | RV32I, Instruction non-specific | | Coverage that need not be crossed with any specific RV32 instruction. | Add coverage to ensure toggles of all bits on all GPRs and all bits of immediates. | Compliance tests: correct test signature.<br>Random tests: RTL matches ISS. | Non-test-specific | Functional coverage of GPR and immediate values. Note that this could also be done with code-coverage, but this will be micro-arch specific. |
| ISA Chapter 2.4 | RV32I Register-Immediate Instructions | ADDI | addi rd, rs1, imm[11:0]<br>rd = rs1 + Sext(imm[11:0])<br>Arithmetic overflow is lost and ignored | Exercise instruction using all combinations of source and destination operands.<br><br>Exercise overflow and underflow. | Compliance tests: correct test signature.<br>Random tests: RTL matches ISS. | Compliance / Random | Test case (Compliance).<br>Functional coverage of verification goals with special attention to **NOP**. |
| | | SLTI | slti rd, rs1, imm[11:0]<br>rd = (rs1 < Sext(imm[11:0]) ? 1 : 0<br>Both imm and rs1 treated as **signed** numbers | Exercise instruction using all combinations of source and destination operands. | Compliance tests: correct test signature.<br>Random tests: RTL matches ISS. | Compliance / Random | Test case (Compliance).<br>Functional coverage of verification goals. |
| | | SLTUI | sltui rd, rs1, imm[11:0]<br>rd = (rs1 < Sext(imm[11:0]) ? 1 : 0 | Exercise instruction using all combinations of source and | Compliance tests: correct test signature. | Compliance / Random | Test case (Compliance).<br>Functional coverage of |

Hierarchically organized:
- one per High-level Feature

- All CORE-V-VERIF DV Plans are open-source artifacts:
  - ...both formal and simulation

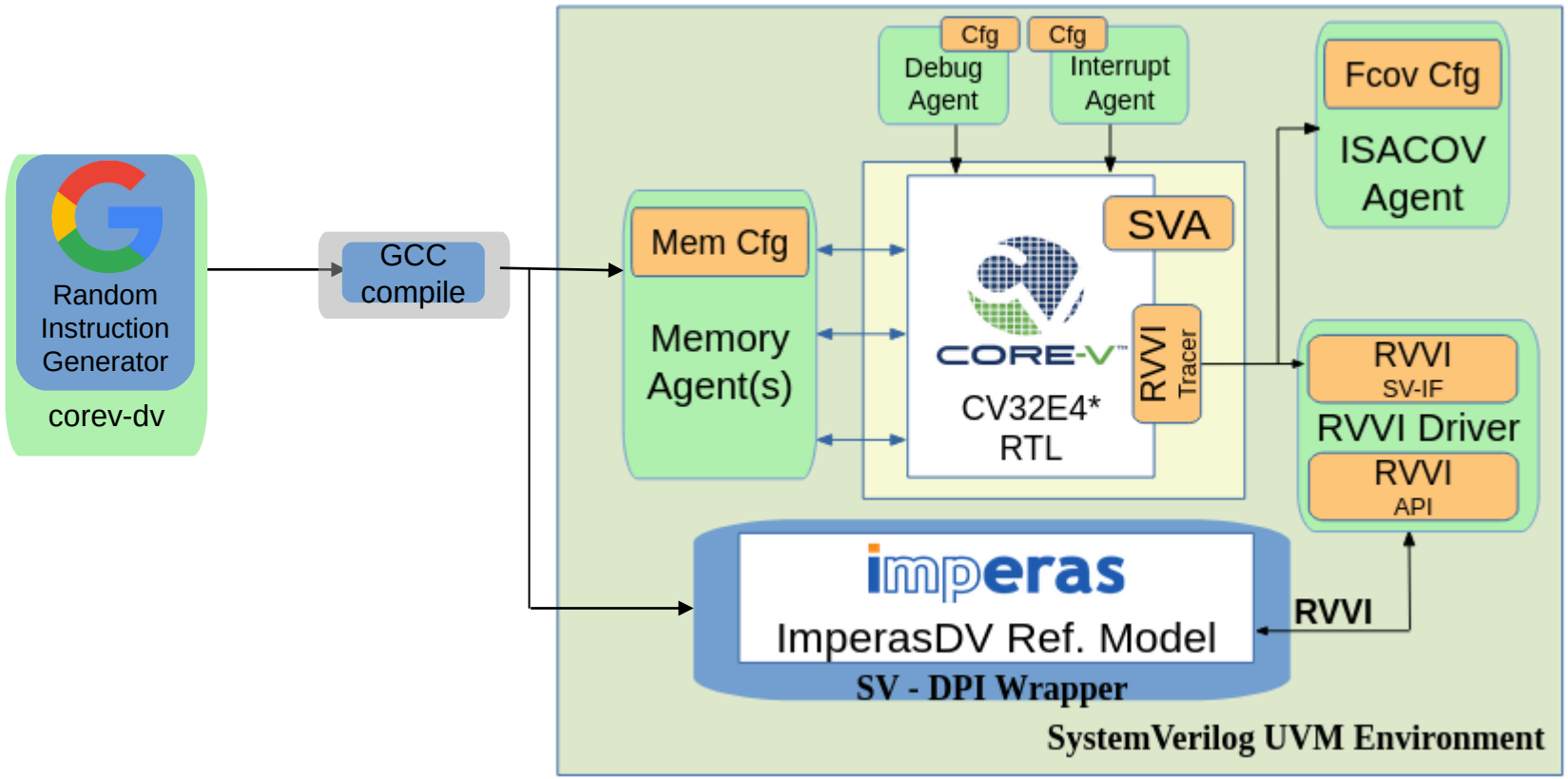
| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | Cover specific case of XORI rd, rs1, -1<br>(bitwise NOT) | ISS. | | |

# "CORE" Testbench




- CORE Testbench capabilities:
  - Demonstration platform
  - RISC-V Compliance

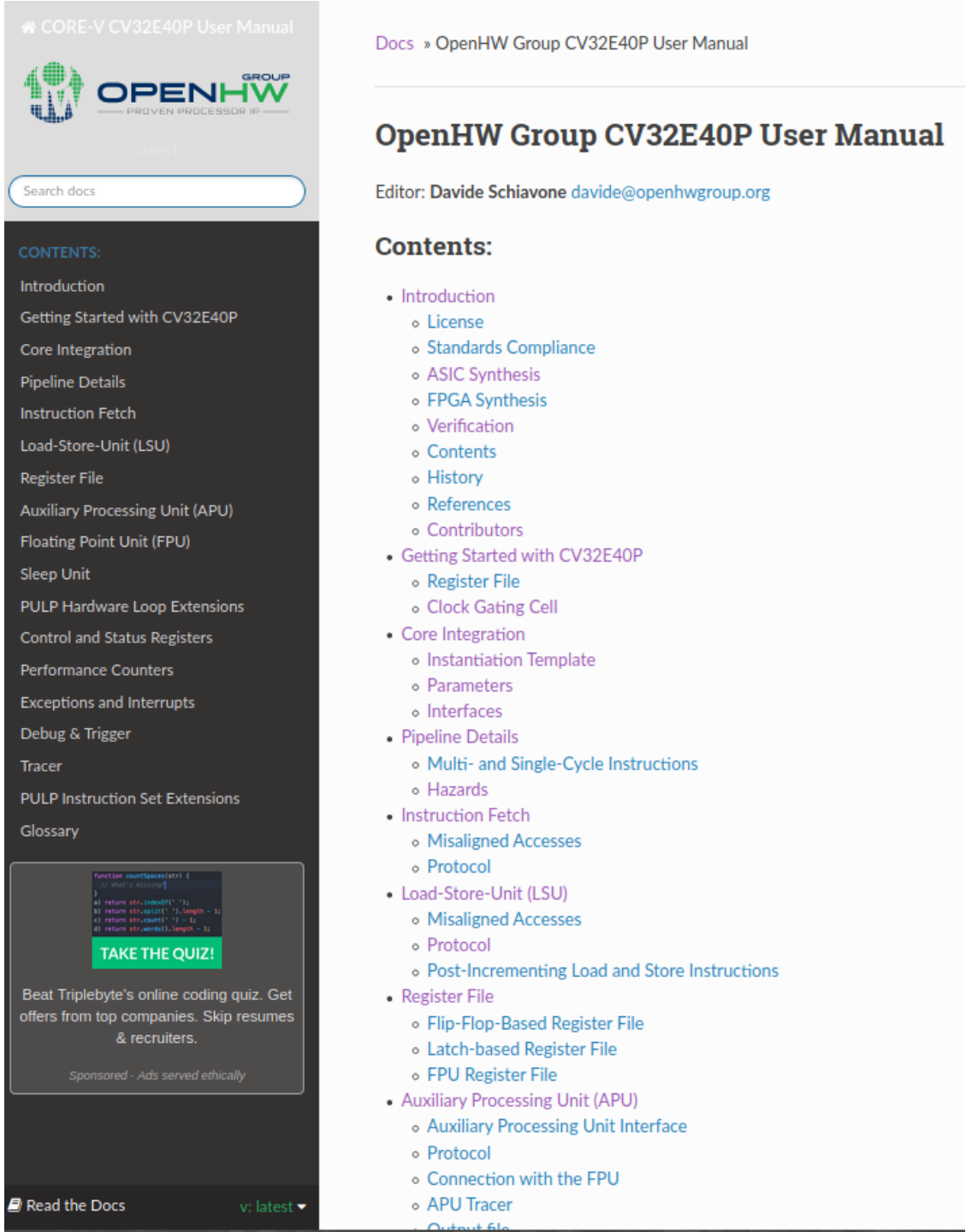
# CORE-V-VERIF UVM Environment




- UVM Environment capabilities:
  - All core testbench capabilities, plus
  - 100% code and functional coverage.

# Is this approach to verification necessary?

- It depends on your goals:
  - For TRL-3 maybe the CORE TB is sufficient.
  - For TRL-5 the bar is higher.
- Released versions of OpenHW IP:
  - Open source, easy to access User Manual on ReadTheDocs.
  - Well structured RTL implementations.
  - Complete verification environment capable of achieving 100% coverage.

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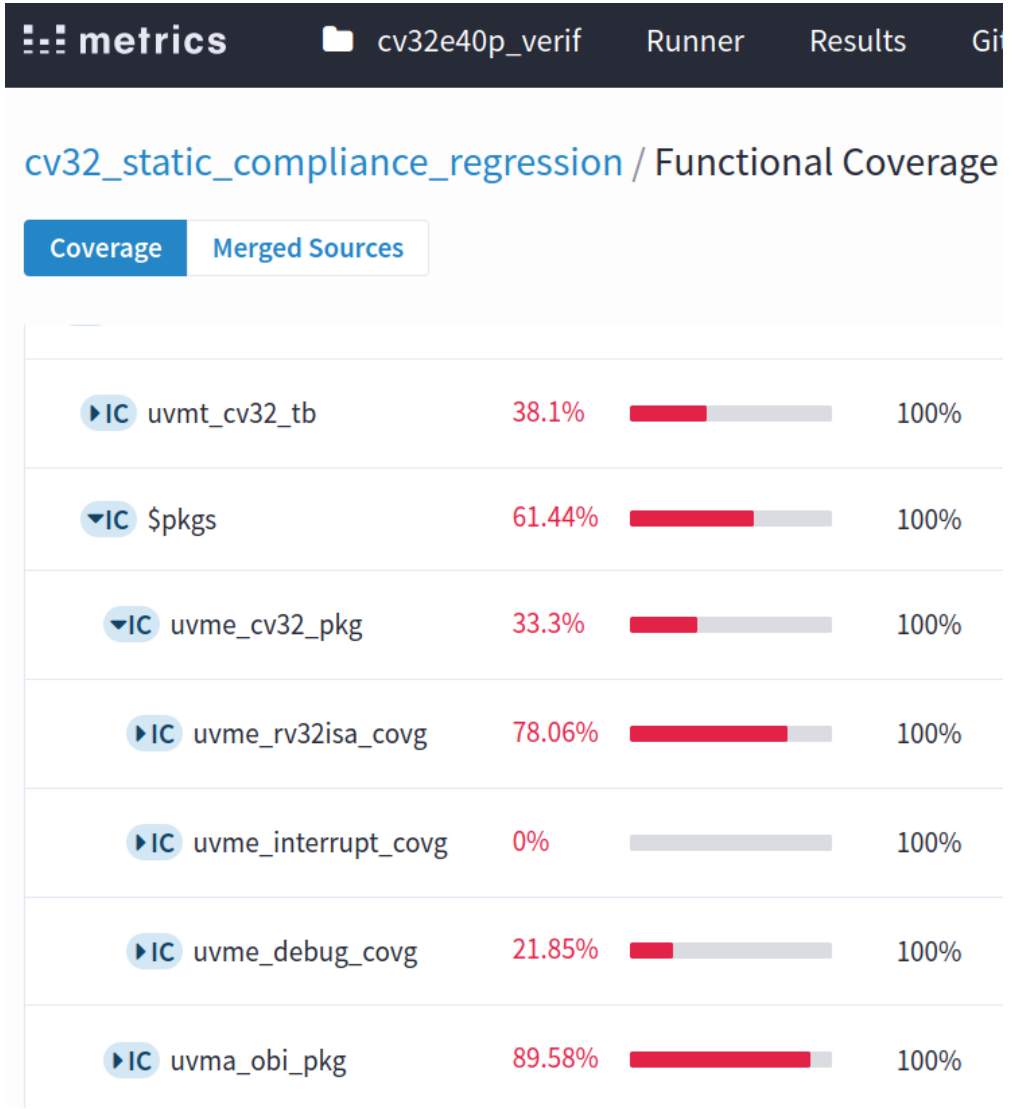
# Why not just run Compliance?

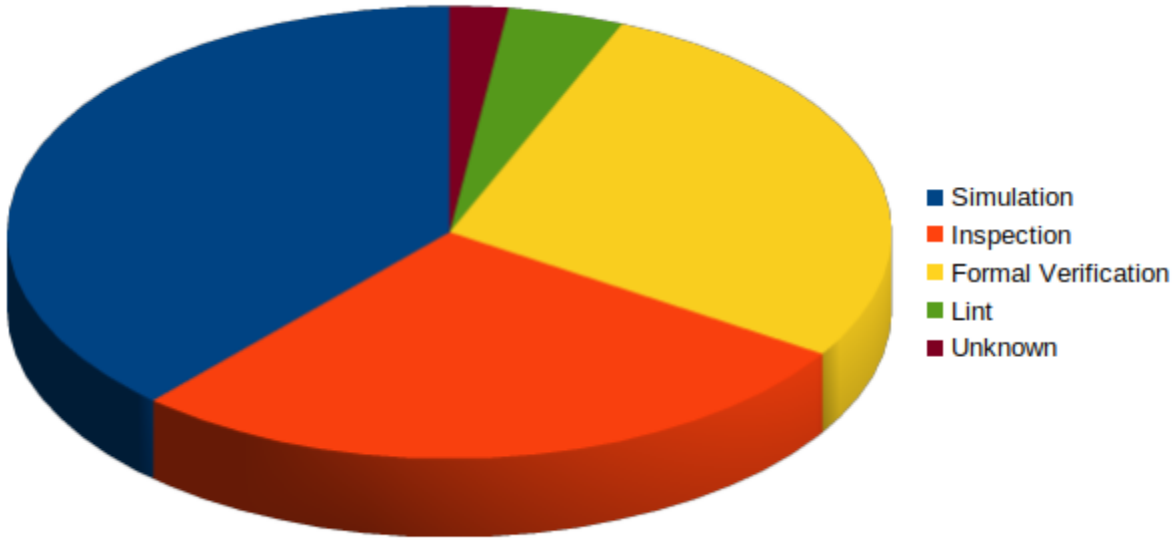
- The RISC-V ISA Compliance Test-Suite is ‘necessary but insufficient’ for complete verification.
- In order to cover all Features in the DV plans, a much more comprehensive verification effort is required:
  - Goals defined by DVplans.
  - Progress measured by coverage.
- None of the 47 bugs we found were triggered by compliance testing.



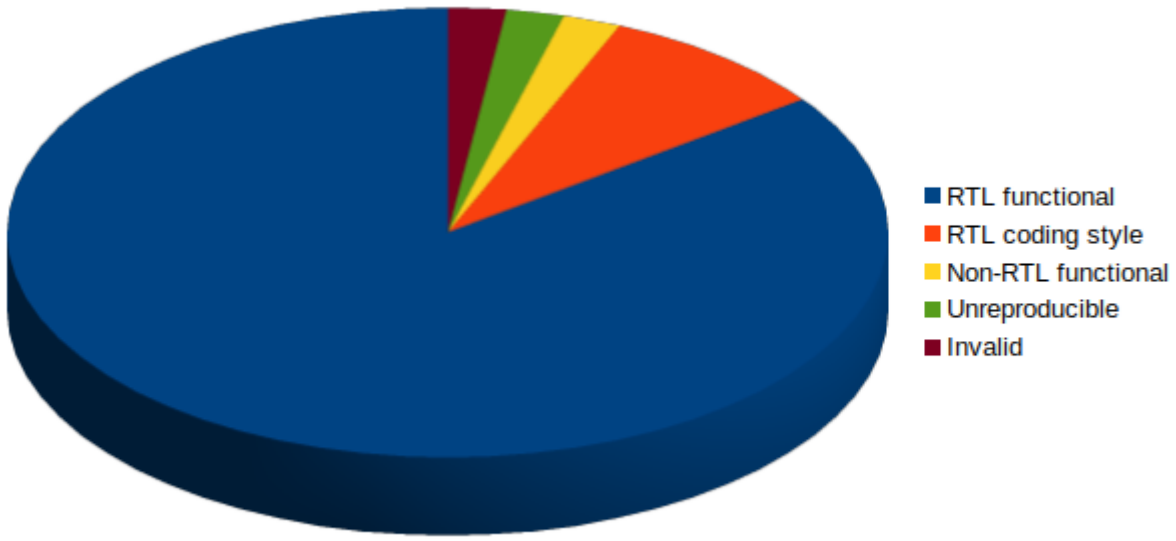
# An Example:
# CV32E40P Verification Results

- The CV32E40P core started its life as the RI5CY core:
  - Known to be high-quality open source implementation.
  - Implemented in silicon multiple times.

- 47 RTL bugs were found.




How Bugs Were Found




Types of Bugs Found

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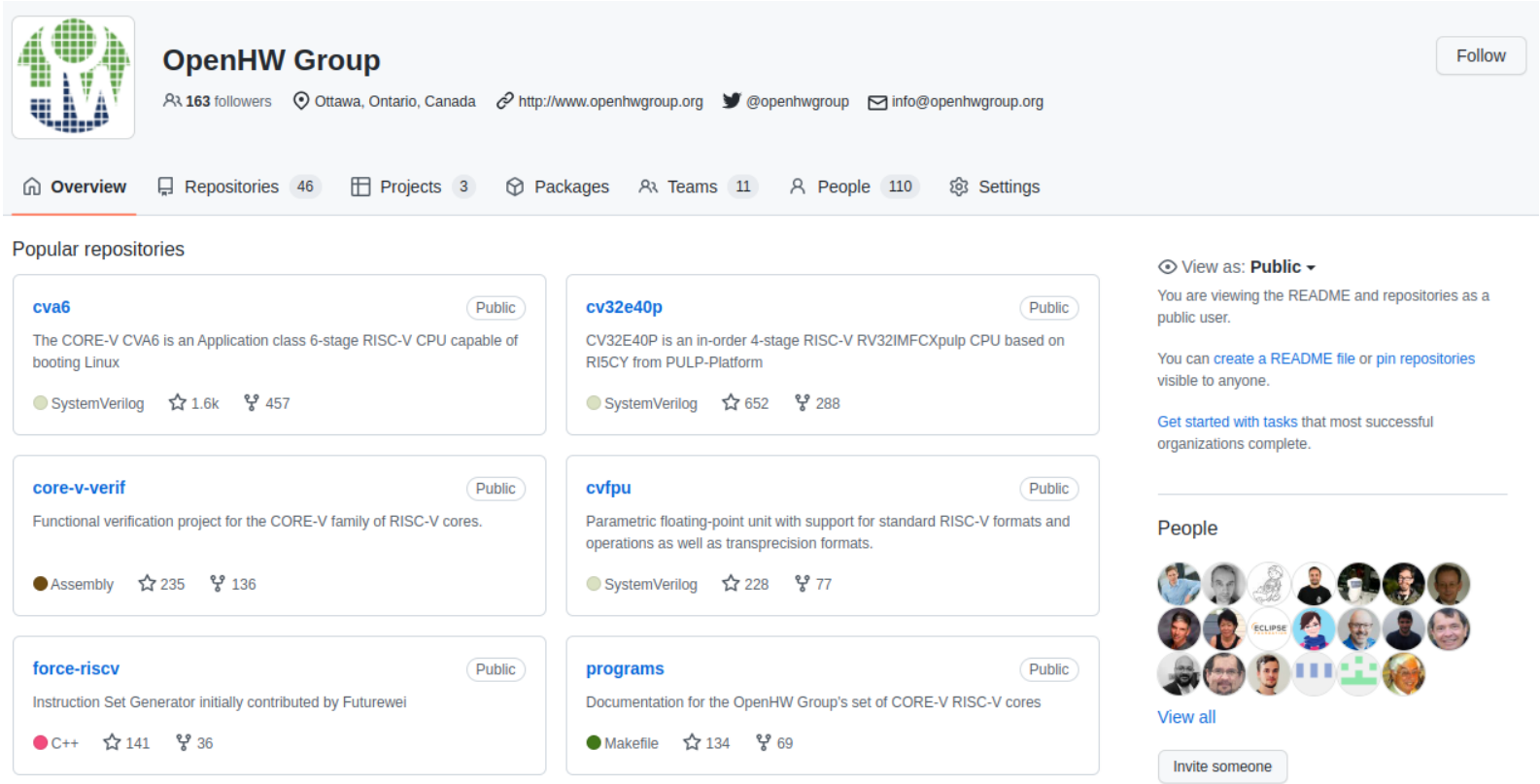
CORE-V™

- OpenHW Group is a not-for-profit, member driven organization collaboratively developing of the CORE-V Family of open-source RISC-V cores.
- We apply Industrial practises to achieve industrial quality results.
- Find us on GitHub!

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# Thank You!